THOMSON
images & beyond

Brian Cromarty
Patent Counsel

May 3, 2010

TO: Mr. Lee, Patent Examiner USPTO

From: Brian J. Cromarty, Patent Counsel

Docket No. PU040057
Serial No. 10/587,757 filed July 28, 2006

Mr. Lee:

This fax is related to our phone conversation of May 3, 2010. Kindly find enclosed the missing pages you requested for this case (pages 10-13).

If you have any other questions please do not hesitate to contact me at (609) 734-6804).

Brian J. Cromarty/nb
Enclosures

television set could also display skewed colors on its screen if the chroma lock is achieved but close tracking is not maintained.

Figure 4 is a flowchart that illustrates an exemplary embodiment of a process of updating a frequency reference in an integrated receiver decoder (140 of Fig. 1). During the startup procedure after being first powered on (410), the IRD will load the stored BRM value from the nonvolatile memory (420). The IRD then applies this BRM value to the VCXO to tune the satellite signal (430). Once the IRD locks in the satellite signal the controller will receive data packets comprising time stamps indicating the time the packets were transmitted from the satellite (445). After at least two of these time stamps are received, the controller calculates a desired BRM value for the VCXO based on the time interval between the two or more of the received time stamps (447) The controller the compares this desired BRM value against the BRM value being applied to the VCXO (450). If the desired value is significantly different from the applied BRM value, the controller stores the desired BRM value in the nonvolatile memory (460), loads this BRM value from the nonvolatile memory (420), and then applies this new BRM value to the VCXO (430). The processes of determining a new BRM value (445), comparison (450) and possible update (460) is then repeated after a predetermined time interval. However, if the desired BRM value is not significantly different from the stored BRM value, the BRM value is not updated and the processes of determining an new BRM value (445), comparison (450) and possible update (460) is then repeated after a predetermined time interval.

Figure 5 shows a flowchart that illustrates an exemplary embodiment of a process of initializing the updating of a frequency reference in an integrated receiver decoder (140 of Fig. 1). After an new BRM value is calculated by the controller, the process of updating the BRM value applied to the VCXO is initiated (510). The controller reads the BRM value from a memory, such as an EEPROM (520). The controller then determines if the BRM value is a valid value (530). If the BRM value is not valid, the controller continues to use the default BRM value (540). If the value is valid, the controller replaces the default BRM value with the calculated BRM value (550). The controller then changes the adjustment state for adjusting the BRM value applied to the VCXO to fine (560). The controller then returns to operational state (570).

Figure 6 shows a flowchart that illustrates an exemplary embodiment of a process of interrupting operation to update the stored BRM value of a frequency reference in an integrated receiver decoder (140 of Fig. 1). After a period of time has elapsed since the previous BRM update, the controller will monitor the incoming data signals until an adaptation packet containing a time stamp is received. After the adaptation packet containing a time stamp is received, the operation of the controller is interrupted (610). An exemplary period of time between BRM updates could be 1 second, but may be longer or shorter depending on the system operational requirements and/or design goals. One the interrupt has been generated, the controller latches the local clock to get a value, called the local clock reference (LCR) in this embodiment, representing the local time when the time stamp in the adaptation field was received (620). Next, the previous controller saves the previously stored LCR into a alternate memory location (630). The controller then stores the new local clock reference to the primary local clock reference memory location (640). The previously stored system clock reference (SCR), calculated from the previously received time stamp in an adaption field is stored to an alternate SCR memory location (650). The newly received SCR is then stored in the primary SCR memory location (660). The controller then checks the appropriate memory value to determine the BRM adjustment state reference variable (670). If the stored state reference variable is equal to rough, the controller executed the rough adjust subroutine (680). If the stored state reference variable is not equal to rough, the controller executed the fine adjust subroutine (690). After the appropriate subroutine is completed, the controller returns to its operational state (695).

Figure 7 shows a flowchart that illustrates an exemplary embodiment of a process of fine adjusting the BRM of a frequency reference in an integrated receiver decoder (140 of Fig. 1). The interrupt routine described in figure 6 or the rough adjust subroutine described in figure 8 initiate the fine adjust subroutine (705). First the controller, decides if an appropriate interval has passed since the last time the BRM value was calibrated (710). If an appropriate time interval has

passed, where in this embodiment the interval is 1 second, a system clock reference delta is calculated by subtracting the previous SCR value from the new SCR value (715). A local clock reference delta is then calculated by subtracting the previous local clock reference value from the new local clock reference value (720). The clock error is then calculated by subtracting the local clock reference delta from the system clock reference delta (725). If the clock error is greater than a predetermined fine adjust threshold, the controller initiates the rough adjust subroutine (735). If the clock error is less than the predetermined fine adjust threshold, the controller then determines if the clock error is greater than the BRM resolution (740). Since the BRM value is a digital value, it has a finite number of values, as described in the description of Fig. 4, in can only be adjusted if the clock error is greater than half of the BRM resolution. In this exemplary embodiment, the BRM value is adjusted if the clock resolution is greater than the BRM resolution (745). If the clock error is less than the BRM resolution value, the BRM value is not adjusted. After the controller adjusts the BRM value or not, the BRM delta is calculated by subtracting the current BRM value from the BRM value stored in memory (750). If the BRM delta value is greater than a previously determined new BRM threshold, the current BRM value is stored in the memory in place of the previous BRM value stored in memory (760). If the BRM delta does is not greater than the new BRM threshold, the controller does not store the current BRM value to the memory and the previous BRM value is retained. The controller then returns to the interrupt subroutine (770).

Figure 8 shows a flowchart that illustrates an exemplary embodiment of a process of rough adjusting the BRM of a frequency reference in an integrated receiver decoder (140 of Fig. 1). The interrupt routine described in figure 6 or the fine adjust routine described in figure 7 can initiate the rough adjust subroutine in this embodiment (805). First the controller, decides if an appropriate interval has passed since the last time the BRM value was calibrated (810). If an appropriate time interval has passed, where in this embodiment the interval is 1 second, a

system clock reference delta is calculated by subtracting the previous SCR value from the new SCR value (815). A local clock reference delta is then calculated by subtracting the previous local clock reference value from the new local clock reference value (820). The clock error is then calculated by subtracting the local clock reference delta from the system clock reference delta (825). If the clock error is greater than a predetermined fine adjust threshold, in this exemplary embodiment the threshold is 0, the controller adjusts the BRM value (835). IF the clock error is less than the clock error threshold the fine adjust subroutine is initiated (850). After the controller adjusts the BRM value, the BRM delta is calculated by subtracting the current BRM value from the BRM value stored in memory (840). If the BRM delta value is less than a previously determined rough threshold the fine adjust subroutine is initiated (850). After the fine adjust subroutine is completed, the subroutine from which the rough adjust subroutine was initiated is returned to (855). If the rough adjust threshold is not exceed, the subroutine from which the rough adjust subroutine was initiated is returned to (855).

While the present invention has been described with reference to the preferred embodiments, it is apparent that various changes may be made in the embodiments without departing from the spirit and the scope of the invention, as defined by the appended claims.